IN THE CLAIMS:

1. (Cancelled) An integrated circuit comprising:

a semiconductor substrate;

a front-end structure coupled to said semiconductor substrate;

a single damascene layer coupled to said front-end structure;

a dual damascene layer coupled to said single damascene layer, said dual damascene layer comprising trenches and vias within a dielectric material; and

a dual damascene pattern liner coupled to said vias.

2. (Cancelled) The integrated circuit of Claim 1 wherein said dielectric material comprises low-k material.

3. (Cancelled) The integrated circuit of Claim 2 wherein said low-k material comprises OSG.

4. (Cancelled) The integrated circuit of Claim 1 wherein said dual damascene pattern liner comprises a refractory metal.

5. (Cancelled) The integrated circuit of Claim 4 wherein said refractory metal comprises TiN.

6. (Cancelled) The integrated circuit of Claim 1 wherein said dual damascene pattern liner comprises a dielectric film.

7. (Cancelled) The integrated circuit of Claim 6 wherein said dielectric film is SiN.

8. (Cancelled) The integrated circuit of Claim 1 wherein said dual damascene pattern liner fully covers a surface of said vias.

9. (Cancelled) The integrated circuit of Claim 1 wherein said dual damascene pattern liner comprises at least two films coupled together.

10. (Cancelled) The integrated circuit of Claim 1 wherein said dual damascene pattern liner comprises a metal film coupled to a dielectric film.

11. (Cancelled) An integrated circuit comprising:

a semiconductor substrate;

a front-end structure coupled to said semiconductor substrate;

a single damascene layer coupled to said front-end structure;

a dual damascene layer coupled to said single damascene layer, said dual damascene layer comprising trenches and vias within a dielectric material; and

a dual damascene pattern liner coupled to said trenches.

12. (Cancelled) The integrated circuit of Claim 11 wherein said dielectric material comprises low-k material.

13. (Cancelled) The integrated circuit of Claim 12 wherein said low-k material comprises OSG.

14. (Cancelled) The integrated circuit of Claim 11 wherein said dual damascene pattern liner comprises a refractory metal.

15. (Cancelled) The integrated circuit of Claim 14 wherein said refractory metal comprises TiN.

16. (Cancelled) The integrated circuit of Claim 11 wherein said dual damascene pattern liner comprises a dielectric film.

17. (Cancelled) The integrated circuit of Claim 16 wherein said dielectric film is SiN.

18. (Cancelled) The integrated circuit of Claim 11 wherein said dual damascene pattern liner comprises at least two films coupled together.

19. (Cancelled) The integrated circuit of Claim 11 wherein said dual damascene pattern liner comprises a metal film coupled to a dielectric film.

20. (Original) A method of manufacturing a semiconductor wafer comprising:

forming a front-end structure over a semiconductor substrate;

forming a single damascene back-end structure metal layer over said front-end structure; and

forming a dual damascene back-end structure over said single damascene back-end structure metal layer, said dual damascene back-end structure comprising:

forming a via etch stop layer over said single damascene back-end structure metal layer;

forming a dielectric layer over said via etch stop layer;

forming a cap layer over said dielectric layer;

forming a non-photoactive layer over said cap layer;

forming a photoresist layer over said non-photoactive layer;

patterning said photoresist layer;

etching via holes;

removing said photoresist layer and said non-photoactive layer;

forming a dual damascene pattern liner over said cap layer and within said via holes;

forming a non-photoactive layer over said dual damascene pattern liner;

forming a photoresist layer over said non-photoactive layer

patterning said photoresist layer; and

etching trench spaces.

21. (Original) The method of Claim 20 wherein said dielectric layer comprises an Inter-Level Dielectric layer and an Inter-Metal Dielectric layer.

22. (Original) The method of Claim 20 wherein said dielectric layer comprises an Inter-Level Dielectric layer, a trench stop layer, and an Inter-Metal Dielectric layer.

23. (Original) The method of Claim 20 wherein said dielectric layer comprises a low-k material.

24. (Original) The method of Claim 20 wherein said step of etching via holes includes etching said via etch stop layer between said via holes and said single damascene back-end structure metal layer.

25. (Original) The method of Claim 20 wherein said step of etching via holes comprises etching partial via holes and then completing an etching of said via holes during said step of etching trench spaces.

26. (Original) The method of Claim 20 further comprising forming at least one additional dual damascene back end structure over said semiconductor substrate.

27. (Original) The method of Claim 20 wherein said step of forming a dual damascene pattern liner comprises forming a multi-layer dual damascene pattern liner.

28. (Original) The method of Claim 27 wherein said multi-layer dual damascene pattern liner comprises at least one metal film and at least one dielectric film.

29. (Original) The method of Claim 20 wherein said dual damascene pattern liner comprises a metal film.

30. (Original) The method of Claim 20 wherein said dual damascene pattern liner comprises a dielectric film.

31. (Original) A method of manufacturing a semiconductor wafer comprising:

forming a front-end structure over a semiconductor substrate;

forming a single damascene back-end structure metal layer over said front-end structure; and

forming a dual damascene back-end structure over said single damascene back-end structure metal layer, said dual damascene back-end structure comprising:

forming a via etch stop layer over said single damascene back-end structure metal layer;

forming a dielectric layer over said via etch stop layer;

forming a cap layer over said dielectric layer;

forming a non-photoactive layer over said cap layer;

forming a photoresist layer over said non-photoactive layer;

patterning said photoresist;

etching trench spaces;

removing said photoresist layer and said non-photoactive layer;

forming a dual damascene pattern liner over said cap layer and within said trench spaces;

forming a non-photoactive layer over said dual damascene pattern liner;

forming a photoresist layer over said non-photoactive layer;

patterning said photoresist layer; and

etching via holes.

32. (Original) The method of Claim 31 wherein said dielectric layer comprises an Inter-Level Dielectric layer and an Inter-Metal Dielectric layer.

33. (Original) The method of Claim 31 wherein said dielectric layer comprises an Inter-Level Dielectric layer, a trench stop layer, and an Inter-Metal Dielectric layer.

34. (Original) The method of Claim 31 wherein said dielectric layer comprises a low-k material.

35. (Original) The method of Claim 31 wherein said step of etching via holes includes etching said via etch stop layer between said via holes and said single damascene back-end structure metal layer.

36. (Original) The method of Claim 31 further comprising forming at least one additional dual damascene back end structure over said semiconductor substrate.

37. (Original) The method of Claim 31 wherein said step of forming a dual damascene pattern liner comprises forming a multi-layer dual damascene pattern liner.

38. (Original) The method of Claim 37 wherein said multi-layer dual damascene pattern liner comprises at least one metal film and at least one dielectric film.

39. (Original) The method of Claim 31 wherein said dual damascene pattern liner comprises a metal film.

40. (Original) The method of Claim 31 wherein said dual damascene pattern liner comprises a dielectric film.

Should the Examiner have any further comments or suggestions, it is respectfully requested that the Examiner contact the undersigned in order to expeditiously resolve any outstanding issues.

Respectfully submitted,

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